Unigen™
Solutions For A Real Time World™

UG51U7211P8DR-BDK-000-00

SYNCHRONOUS DRAM MODULE

4G Bytes (512M x 72 bits)

240 Pin PC3-10600 DDR3 SDRAM Register & PLL DIMM w/ECC

based on 9 pcs 512M x 8 DDR3 SDRAM 8K Refresh

Specifications

- RoHS Compliant (Lead Free) Memory module
- Density: 4GB
- Organization
  — 512M x 72 bits, 1 Rank
- Mounting 9 pieces of 4G bits DDR3 SDRAM sealed In FBGA
- Package: 240-pin socket type registered dual in line memory module (DIMM)
  — PCB height: 18.75mm
- VDD = 1.35V (1.283 to 1.45V)
- Backward Compatible with 1.5V DDR3 environment
- VDDSPD = +3.0V to +3.6V
- Fast Data Transfer Rate: PC3-12800
- Serial Presence-Detect (SPD)with EEPROM
- Eight Internal banks for concurrent operation (components)
- On-Die-Termination (ODT) for better signal quality
- Interface: SSTL_15
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- CAS (READ) latency (CL): 5, 6, 7, 8, 9, 10, 11
- POSTED CAS ADDITIVE latency (AL)
- Precharge: Auto precharge option for each burst access
- Refresh: Auto-refresh, self-refresh
- Average refresh cycle
  — 7.8µs at 0°C~85°C
  — 3.9µs at 85°C~95°C
- Operating case temperature range
  — TC = 0°C~95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by progrmmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  — Synchronous ODT
  — Dynamic ODT
  — Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ON-Die-Termination
- Progrmmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- Extended Self-Refresh
  — External Self-Refresh
  — Auto Self-Refresh

PART IDENTIFICATION

PART NO.	REF. CYCLE	SDRAM PACKAGE	PLATING
UG51U7211P8DR	8K	FBGA	Gold

SPEED INFORMATION

Module Marking	CAS Latency	SPEED	
-BDK	CL11	1.25ns	1600MHz

REVISION HISTORY

Mar 18 , 2014

Rev - C Product brief released.

PIN CONFIGURATIONS

240-pin DDR3 RDIMM ECC Front								240-pin DDR3 RDIMM ECC Back							
Pin	symbol	Pin	symbol	Pin	symbol	Pin	symbol	Pin	symbol	Pin	symbol	Pin	symbol	Pin	symbol
	REFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3/ TDQS12	182	VDD	212	DM5/ TDQS14
3	DQ0	33	DQS3#	63	NC	93	DQS5#	123	DQ5	153	NF/ TDQS12#	183	VDD	213	NF/ TDQS14#
4	DQ1	34	DQS3	64	NC	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0/ TDQS9	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	VDD	96	DQ42	126	NF/ TDQS9#	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	NC	217	VSS
8	VSS	38	VSS	68	Par_In	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	DM8/ TDQS17	191	VDD	221	DM6/ TDQS15
12	DQ8	42	DQS8#	72	VDD	102	DQS6#	132	DQ13	162	NF/ TDQS17#	192	RAS#	222	NF/ TDQS15#
13	DQ9	43	DQS8	73	WE#	103	DQS6	133	VSS	163	VSS	193	S0#	223	VSS
14	VSS	44	VSS	74	CAS#	104	VSS	134	DM1/ TDQS10	164	CB6	194	VDD	224	DQ54
15	DQS1#	45	CB2	75	VDD	105	DQ50	135	NF/ TDQS10#	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	S1#	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	NC	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	VTT	78	VDD	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	VTT	79	NC	109	DQ57	139	VSS	169	NC	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7/ TDQS16
21	DQ16	51	VDD	81	DQ32	111	DQS7#	141	DQ21	171	NC	201	DQ37	231	NF/ TDQS16#
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	Err_Out#	83	VSS	113	VSS	143	DM2/ TDQS11	173	VDD	203	DM4/ TDQS13	233	DQ62
24	DQS2#	54	VDD	84	DQS4#	114	DQ58	144	NF/ TDQS11#	174	A12	204	NF/ TDQS13#	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

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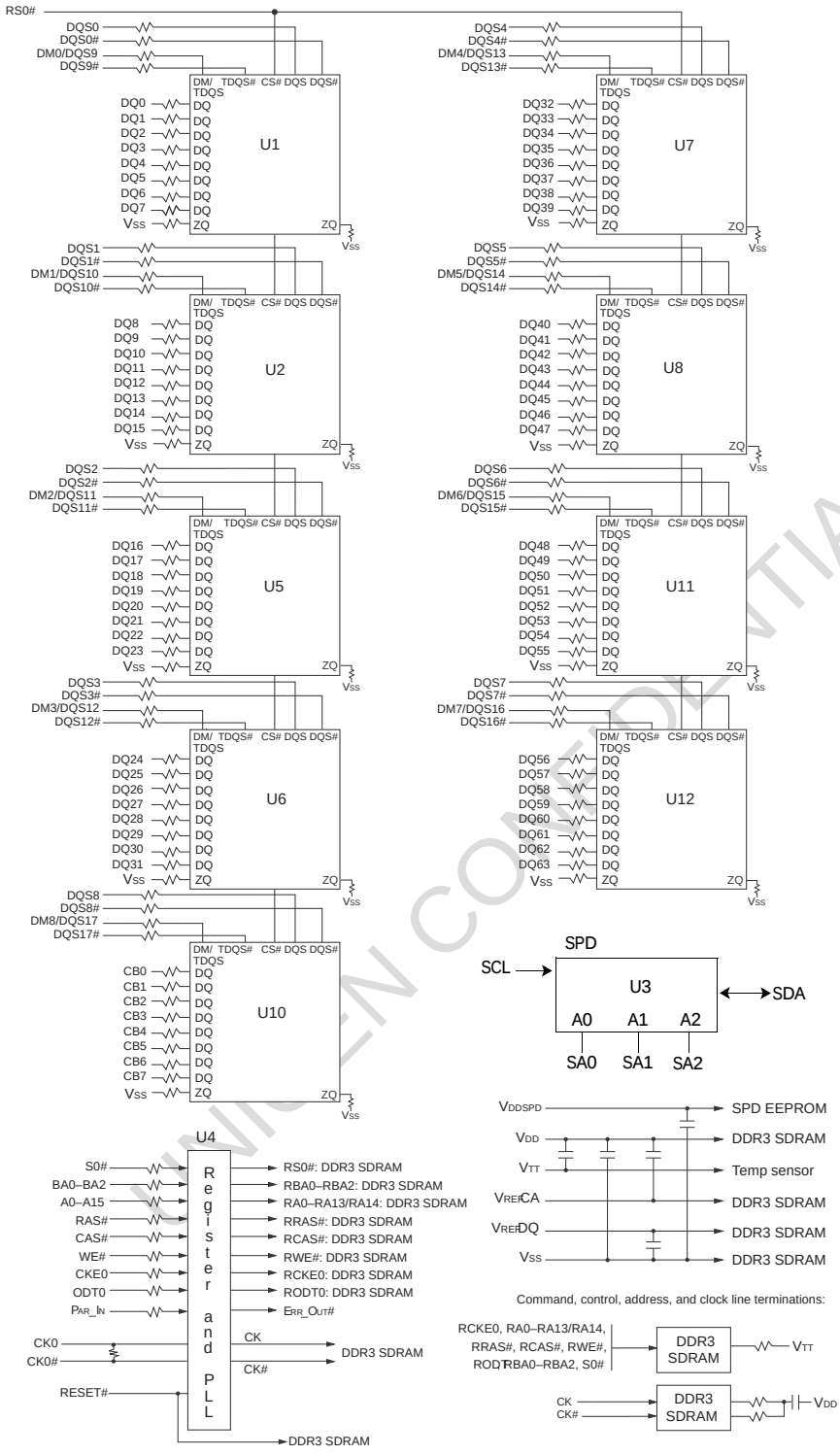
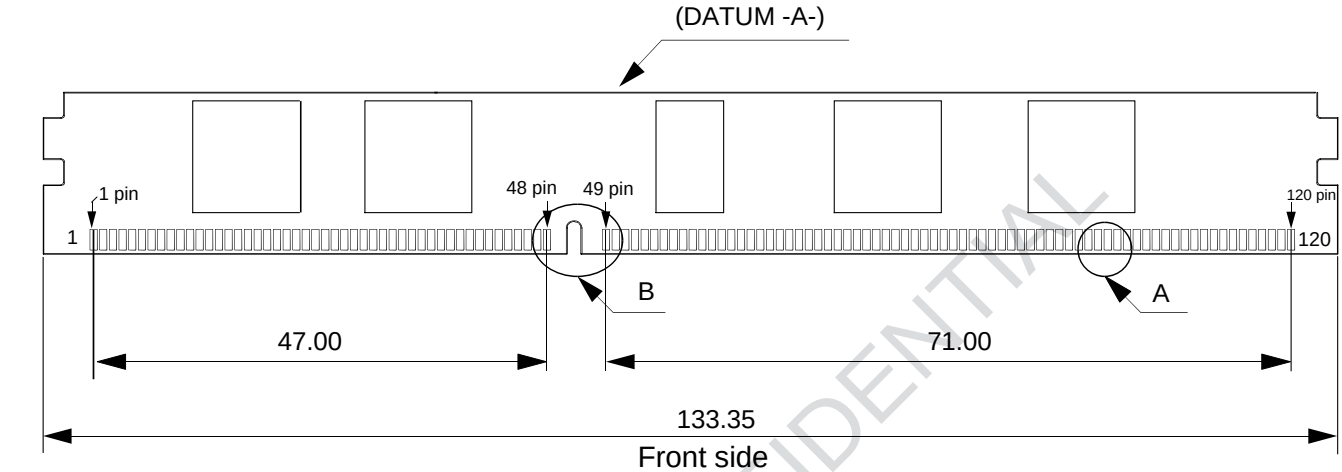
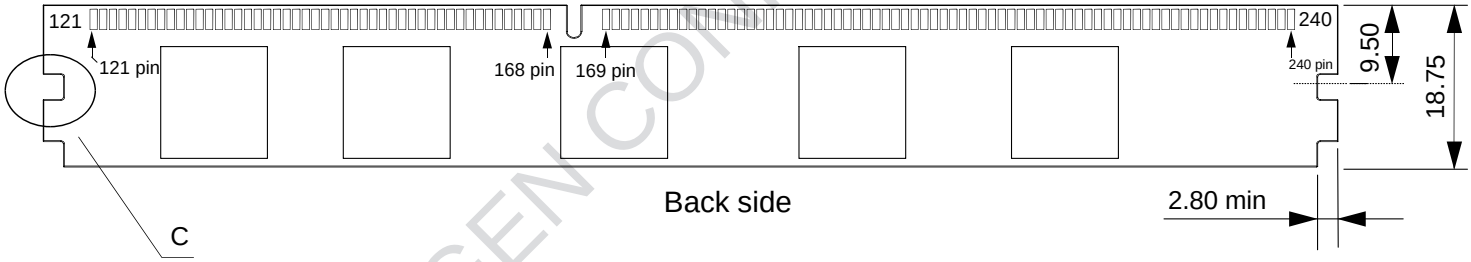
FUNCTIONAL BLOCK DIAGRAM

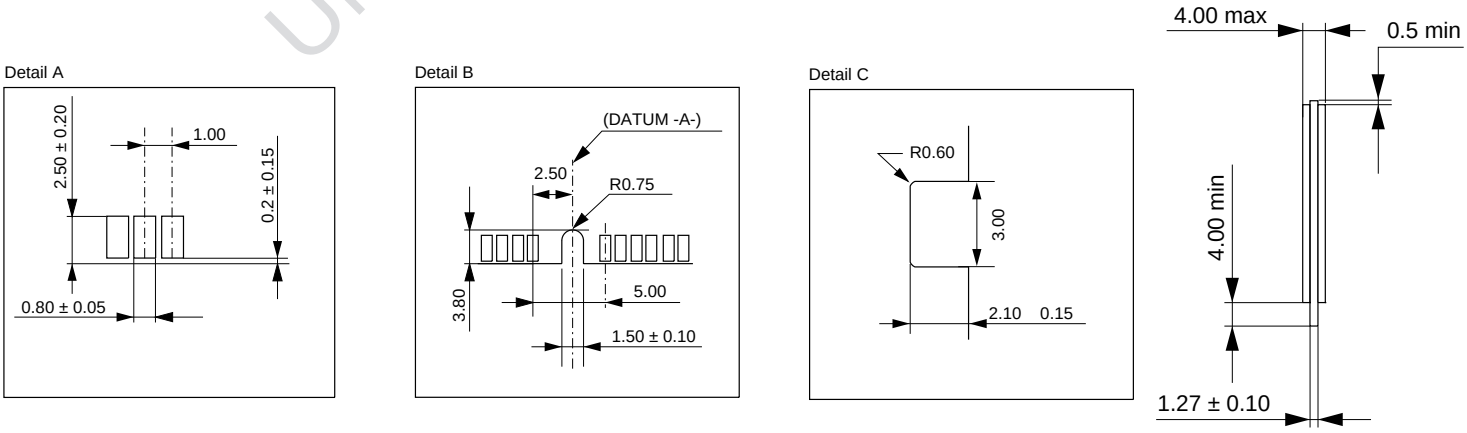


Notes:1.The ZQ ball on each DDR3 component is connected to an external 240 Ohm ±1 percent resistor
X that is tied to ground. It is used for the calibration of the component's ODT and output driver.

PHYSICAL DIMENSION (USING H5TC4G83AFR-PBA) Hynix BRAND







Tolerances : ± 0.127 unless otherwise specified

Units : mm

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